TPSM8282x 1-A and 2-A High Efficiency Step-Down Converter MicroSiP™ Power Module with Integrated Inductor

1 Features

- Low profile MicroSiP™ power module
- Up to 95% efficiency
- 2.4-V to 5.5-V input voltage range
- 0.6-V to 4-V adjustable output voltage
- 4-µA operating quiescent current
- DCS-control topology
- Power save mode for light load efficiency
- 100% duty cycle for lowest dropout
- Hiccup short circuit protection
- Output discharge
- Power good output
- Integrated soft startup
- Overtemperature protection
- 2.0-mm x 2.5-mm x 1.1-mm 10-Pin µSiL package
- 29mm^2 total solution size

2 Applications

- Optical modules
- Machine vision
- Embedded camera system
- Patient monitoring and diagnostics

3 Description

The TPSM8282x device family consists of a 1-A and 2-A step-down converter MicroSiP™ power module optimized for small solution size and high efficiency.

The power modules integrate a synchronous step-down converter and an inductor to simplify design, reduce external components and save PCB area. The low profile and compact solution is suitable for automated assembly by standard surface mount equipment.

To maximize efficiency, the converter operates in PWM mode with a nominal switching frequency of 4MHz and automatically enters Power Save Mode operation at light load currents.

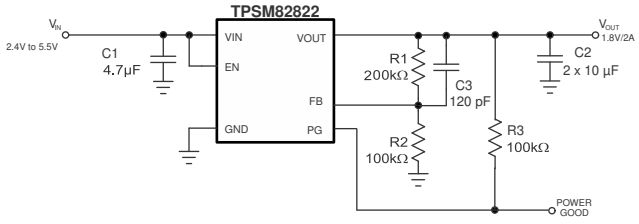
In Power Save Mode, the device operates with typically 4-µA quiescent current. Using the DCS-Control topology, the device achieves excellent load transient performance and accurate output voltage regulation. The EN and PG pins, which support sequencing configurations, bring a flexible system design. An integrated soft startup reduces the inrush current required from the input supply. Over temperature protection and hiccup short circuit protection deliver a robust and reliable solution.

Device Information

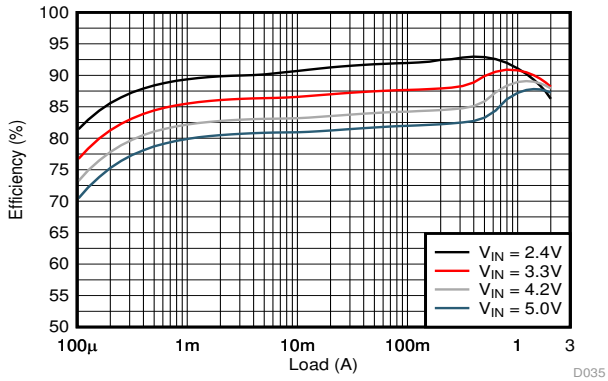
PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPSM82821SIL	µSiL (10)	2.0 mm x 2.5 mm
TPSM82822SIL	µSiL (10)	2.0 mm x 2.5 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.8-V Output Application



1.8-V Output Efficiency



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4 Revision History

Changes from Original (August 2019) to Revision A **Page**

- Change device status from Advance Information to Production Data ... 1
- Added planned device spins to Device Comparison Table ... 3

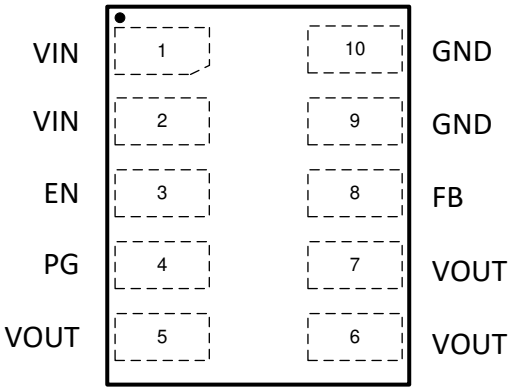
5 Device Comparison Table

DEVICE NUMBER (1)	OUTPUT CURRENT	OUTPUT VOLTAGE
TPSM82821SIL	1 A	adjustable
TPSM82822SIL	2 A	adjustable

(1) For all available packages, see the orderable addendum at the end of the data sheet.

6 Pin Configuration and Functions

µSiL Package
(Top View)



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
EN	3	I	Device enable pin. To enable the device, this pin needs to be pulled high. Pulling this pin low disables the device. Do not leave floating.
FB	8	I	Feedback pin. This pin must be connected to the center of the output voltage resistor divider.
GND	9, 10	PWR	Ground pin.
PG	4	O	Power good open drain output pin. The pull-up resistor can be connected to voltages up to 5.5 V. If unused, leave it floating.
VIN	1, 2	PWR	Input voltage pin.
VOUT	5, 6, 7	PWR	Output voltage pin.

7 Specifications

7.1 Absolute Maximum Ratings(1)

		MIN	MAX	UNIT
Voltage at pins(2)	EN, PG, VIN, FB, VOUT	-0.3	6	V
Module operating temperature range		-40	125	°C
Storage temperature range		-40	125	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommend Operating Conditions

		MIN	MAX	UNIT
V_{IN}	Input voltage range	2.4	5.5	V
V_{PG}	Power good pull-up resistor voltage		5.5	V
V_{OUT}	Output voltage range	0.6	4	V
I_{SINK_PG}	Sink current at PG pin		1	mA
I_{OUT}	TPSM82821 Output current range(1)	0	1	A
I_{OUT}	TPSM82822 Output current range(1)	0	2	A
T_J	Module operating temperature range(1)	-40	125	°C

(1) The module operating temperature range includes module self temperature rise and IC junction temperature rise. In applications where high power dissipation is present, the maximum operating temperature or maximum output current must be derated.

7.4 Thermal Information

THERMAL METRIC(1)		µSiL (JEDEC 51-7) 10-Pin	TPSM82822EVM-080	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	92.5	63.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.3	n/a(2)	
$R_{\theta JB}$	Junction-to-board thermal resistance	27.9	n/a(2)	
ψ_{JT}	Junction-to-top characterization parameter	11.8	9.6	
ψ_{JB}	Junction-to-board characterization parameter	27.5	27.0	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953
(2) Not applicable to an EVM.

7.5 Electrical Characteristics

T_J = –40°C to 125°C and V_{IN} = 2.4 V to 5.5 V. Typical values are at T_J = 25°C and V_{IN} = 5 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
I_Q	Quiescent current into VIN	EN = High, no load, device not switching		4	10	µA
I_{SD}	Shutdown current into VIN	EN = Low, T_J = -40°C to 85°C		0.05	0.5	µA
V_{UVLO}	Under voltage lock out threshold	V_{IN} falling	2.1	2.2	2.3	V
	Under voltage lock out hysteresis	V_{IN} rising		160		mV
T_{JSD}	Thermal shutdown threshold	T_J rising		150		°C
	Thermal shutdown hysteresis	T_J falling		20		°C
LOGIC INTERFACE EN						
V_{IH}	High-level input voltage		1.0			V
V_{IL}	Low-level input voltage				0.4	V
$I_{lkg(EN)}$	Input leakage current into EN pin	EN = High		0.01	0.1	µA
SOFT START, POWER GOOD						
t_{SS}	Soft start time	Time from EN high to 95% of V_{OUT} nominal		1.25		ms
V_{PG}	Power good lower threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	94	96	98	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	90	92	94	%
	Power good upper threshold	V_{PG} rising, V_{FB} referenced to V_{FB} nominal	103	105	107	%
		V_{PG} falling, V_{FB} referenced to V_{FB} nominal	108	110	112	%
$V_{PG,OL}$	Low-level output voltage	I_{sink} = 1mA			0.4	V
$I_{lkg(PG)}$	Input leakage current into PG pin	V_{PG} = 5V		0.01	0.1	µA
OUTPUT						
V_{FB}	Feedback regulation voltage	PWM mode	594	600	606	mV
$I_{lkg(FB)}$	Feedback input leakage current	V_{FB} = 0.6 V		0.01	0.05	µA
i_{DIS}	Output discharge current	EN = Low, V_{OUT} = 0.4V	75	400		mA
POWER SWITCH						
$R_{DS(on)}$	High-side FET on-resistance			26		mΩ
	Low-side FET on-resistance			26		mΩ
R_{DP}	Dropout resistance	TPSM82821, 100% mode. V_{IN} = 2.7V, T_J = 25°C		115	145	mΩ
R_{DP}	Dropout resistance	TPSM82822, 100% mode. V_{IN} = 2.7V, T_J = 25°C		90	120	mΩ
I_{LIMF}	High-side FET switch current limit	TPSM82821	1.75	2.2	2.75	A
I_{LIMF}	High-side FET switch current limit	TPSM82822	2.7	3.3	3.9	A
f_{SW}	PWM switching frequency	I_{OUT} = 1 A		4		MHz

8 Typical Characteristics

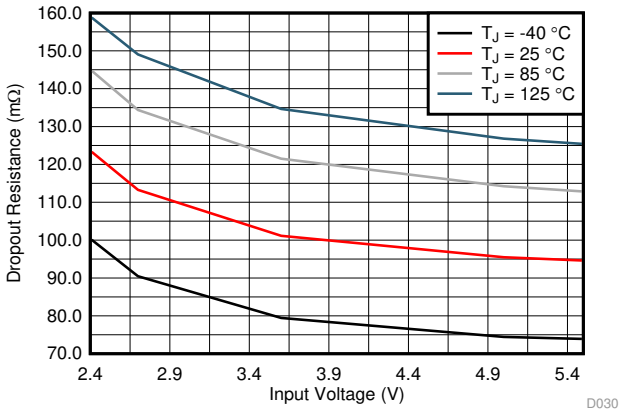


Figure 1. TPSM82821 Dropout Resistance

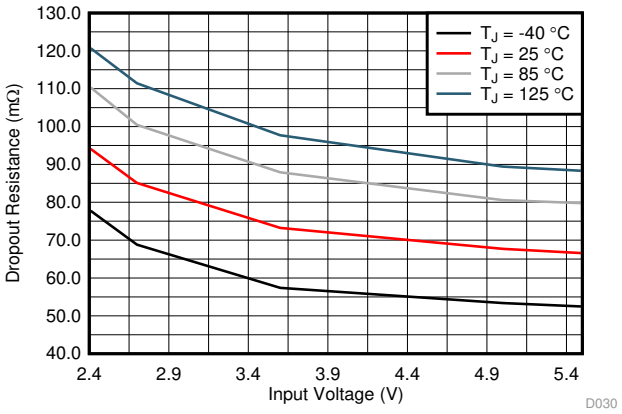


Figure 2. TPSM82822 Dropout Resistance

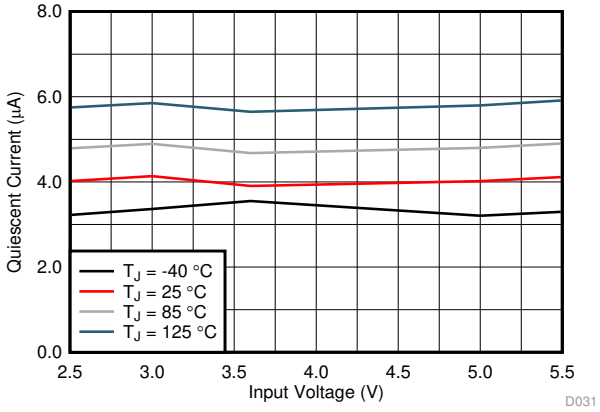


Figure 3. Quiescent Current

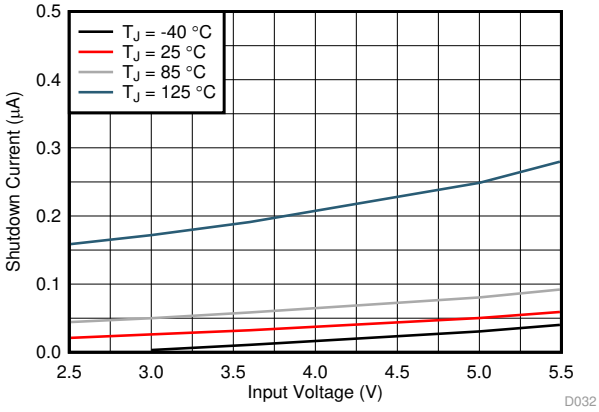


Figure 4. Shutdown Current

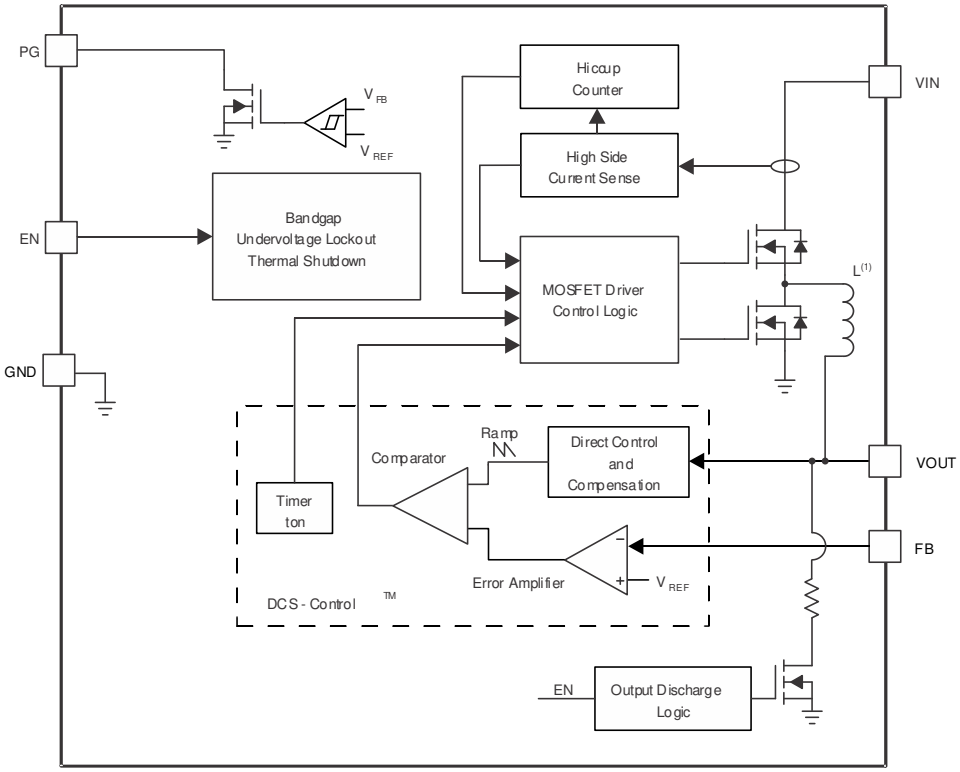
9 Detailed Description

9.1 Overview

The TPSM8282x synchronous step-down converter power module is based on DCS-Control™ (Direct Control with Seamless transition into Power-Save Mode). This is an advanced regulation topology that combines the advantages of hysteretic, voltage and current mode control.

The DCS-Control™ topology operates in PWM (Pulse Width Modulation) mode for medium to heavy load conditions and in PSM (Power-Save Mode) at light load currents. In PWM, the converter operates with its nominal switching frequency of 4 MHz having a controlled frequency variation over the input voltage range. As the load current decreases, the converter enters Power-Save Mode, reducing the switching frequency and minimizing the IC's quiescent current to achieve high efficiency over the entire load current range. DCS-Control™ supports both operation modes using a single building block and therefore has a seamless transition from PWM to PSM without effects on the output voltage. The TPSM8282x offers excellent DC voltage regulation and load transient regulation, combined with low output voltage ripple, minimizing interference with RF circuits.

9.2 Functional Block Diagram



(1) Inductance value is 0.47 µH in TPSM82821 and 0.24 µH in TPSM82822.

9.3 Feature Description

9.3.1 PWM and PSM Operation

The TPSM8282x includes a fixed on-time (t_{ON}) circuitry. This t_{ON}, in steady-state operation in PWM and PSM modes, is estimated as:

$$t_{ON} = 250ns \times \frac{V_{OUT}}{V_{IN}} \quad (1)$$

Feature Description (continued)

In PWM mode, the TPSM8282x operates with pulse width modulation in continuous conduction mode (CCM) with a t_{ON} shown in Equation 1 at medium and heavy load currents. A PWM switching frequency of typically 4MHz is achieved by this t_{ON} circuitry.

To maintain high efficiency at light loads, the device enters Power-Save Mode seamlessly when the load current decreases. This happens when the load current becomes smaller than half the inductor's ripple current. In PSM, the converter operates with a reduced switching frequency and with a minimum quiescent current to maintain high efficiency. The on-time in PSM is also based on the same t_{ON} circuitry. The switching frequency in PSM is estimated as:

$$f_{PSM} = \frac{2 \times I_{OUT}}{t_{ON}^2 \times \frac{V_{IN}}{V_{OUT}} \times \frac{V_{IN} - V_{OUT}}{L}} \quad (2)$$

In PSM, the output voltage rises slightly above the nominal output voltage in PWM mode. This effect is reduced by increasing the output capacitance.

9.3.2 Low Dropout Operation (100% Duty Cycle)

The device offers a low input to output voltage differential by entering 100% duty cycle mode. In this mode, the high-side MOSFET switch is constantly turned on. This is particularly useful in battery powered applications to achieve longest operation time by taking full advantage of the whole battery voltage range. The minimum input voltage to maintain a minimum output voltage is given by:

$$V_{IN(min)} = V_{OUT(min)} + I_{OUT} \times R_{DP} \quad (3)$$

Where

R_{DP} = Resistance from V_{IN} to V_{OUT}, including high-side FET on-resistance and DC resistance of the inductor.

$V_{OUT(min)}$ = Minimum output voltage the load can accept.

9.3.3 Soft Startup

After enabling the device, there is a 250µs delay before switching starts. Then, an internal soft startup circuitry ramps up the output voltage which reaches nominal output voltage during the startup time of 1ms. This avoids excessive inrush current and creates a smooth output voltage rise slope. It also prevents excessive voltage drops of primary cells and rechargeable batteries with high internal impedance.

The device is able to start into a pre-biased output capacitor. It starts with the applied bias voltage and ramps the output voltage to its nominal value.

9.3.4 Switch Current Limit and Hiccup Short Circuit Protection

The switch current limit prevents the device from high inductor current and from drawing excessive current from the battery or input voltage rail. Excessive current might occur with a shorted or saturated inductor or a heavy load or shorted output circuit condition. If the inductor current reaches the threshold of I_{LIMF} the high-side MOSFET is turned off and the low-side MOSFET remains off, while the inductor current flows through its body diode and quickly ramps down.

When this switch current limit is triggered 32 times, the device stops switching. The device then automatically starts a new start-up after a typical delay time of 128 µs has passed. This is named HICCUP short-circuit protection. The device repeats this mode until the high load condition disappears.

9.3.5 Undervoltage Lockout

To avoid mis-operation of the device at low input voltages, under voltage lockout is implemented that shuts down the device at voltages lower than V_{UVLO}.

9.3.6 Thermal Shutdown

The device goes into thermal shutdown and stops the power stage switching when the junction temperature exceeds T_{JSD}. When the device temperature falls below the threshold by 20°C, the device returns to normal operation automatically by switching the power stage again.

9.4 Device Functional Modes

9.4.1 Enable and Disable

The device is enabled by setting the EN pin to a logic high. Accordingly, shutdown mode is forced if the EN pin is pulled low with a shutdown current of typically 50nA. In shutdown mode, the internal power switches as well as the entire control circuitry are turned off. An internal switch smoothly discharges the output through the VOUT pin in shutdown mode. Do not leave the EN pin floating.

The typical threshold value of the EN pin is 0.89V for rising input signal, and 0.62V for falling input signal.

9.4.2 Output Discharge

The purpose of the output discharge function is to ensure a defined down-ramp of the output voltage when the device is disabled and to keep the output voltage close to 0 V. The output discharge is active when the EN pin is set to a logic low and during thermal shutdown. The discharge is not active in UVLO.

9.4.3 Power Good Output

The device has a power good output. The PG pin goes high impedance once the FB pin voltage is above 96% and less than 105% of the nominal voltage, and is driven low once the voltage falls below typically 92% or higher than 110% of the nominal voltage. Table 1 shows the typical PG pin logic.

The PG pin is an open-drain output and is specified to sink up to 1mA. The power good output requires a pull-up resistor connecting to any voltage rail less than 5.5V. The PG signal can be used for sequencing of multiple rails by connecting it to the EN pin of other converters. Leave the PG pin unconnected when not used.

The PG rising edge has a 100 µs blanking time and the PG falling edge has a deglitch delay 20us.

Table 1. PG Pin Logic

DEVICE CONDITIONS		LOGIC STATUS	
		HIGH IMPEDANCE	LOW
Enable	EN = High, $V_{FB} \le 0.552$ V		√
	EN = High, $0.576 \text{ V} \le V_{FB} \le 0.63$ V	√	
	EN = High, $V_{FB} \ge 0.66$ V		√
Shutdown	EN = Low		√
Thermal Shutdown	$T_J > T_{JSD}$		√
UVLO	$0.7 \text{ V} < V_{IN} < V_{UVLO}$		√
Power Supply Removal	$V_{IN} < 0.7$ V	undefined	

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TPSM8282x is a synchronous step-down converter power module whose output voltage is adjusted by component selection. The following section discusses the design of the external components to complete the power supply design. The required power inductor is integrated inside the TPSM8282x. The inductor is shielded and has an inductance of 0.47 µH for the TPSM82821 and 0.24 µH for the TPSM82822, with a +/- 20% tolerance. The TPSM82821 and TPSM82822 are pin-to-pin and BOM-to-BOM compatible.

10.2 Typical Applications

10.2.1 1.8-V Output Application

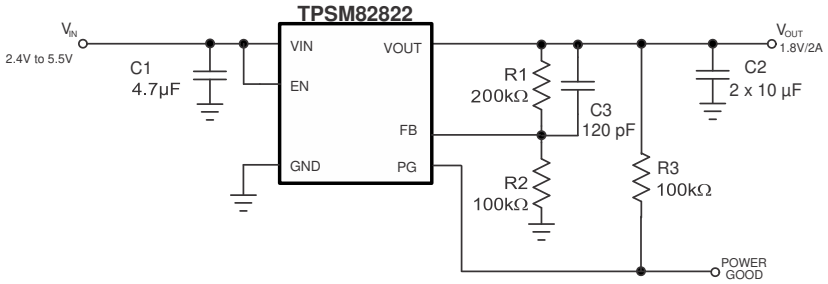


Figure 5. 1.8-V Output Application

10.2.1.1 Design Requirements

For this design example, use the input parameters shown in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	2.4V to 5.5V
Output voltage	1.8V
Output ripple voltage	< 20mV
Output current rating	2A

Table 3 lists the components used for the example.

Table 3. List of Components

REFERENCE	DESCRIPTION	MANUFACTURER
C1	Ceramic capacitor, 4.7-µF, 6.3 V, X7R, size (0603), JMK107BB7475MA	Taiyo Yuden
C2	Ceramic capacitor, 10-µF , 10 V, X7R, size (0603), GRM188Z71A106MA73D	muRata
C3	Ceramic capacitor, 120-pF , 50 V, size (0603), GRM1885C1H121JA01D	muRata
R1	Resistor, 200-kΩ, 1% accuracy	std
R2	Resistor, 100 kΩ, 1% accuracy	std
R3	Resistor, 100 kΩ, 1% accuracy	std

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Setting the Output Voltage

Choose resistors R1 and R2 to set the output voltage within a range of 0.6-V to 4-V, according to Equation 4. To keep the feedback (FB) net robust from noise, set R2 equal to or lower than 100kΩ to have at least 3µA of current in the voltage divider. Lower values of FB resistors achieve better noise immunity, and lower light load efficiency, as explained in SLYT469.

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right) = R2 \times \left(\frac{V_{OUT}}{0.6V} - 1 \right) \quad (4)$$

10.2.1.2.2 Feedforward capacitor

A feedforward capacitor (C_3) is recommended in parallel with R1. Equation 5 calculates the C_3 value.

$$C3 = \frac{12\mu s}{R2} \quad (5)$$

10.2.1.2.3 Input and Output Capacitor Selection

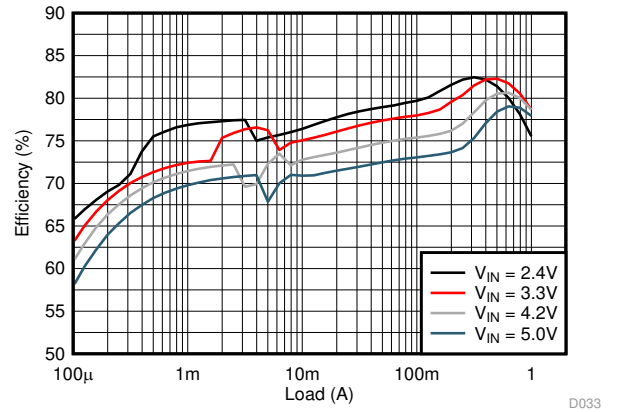
For best output and input voltage filtering, ceramic capacitors are required. The input capacitor minimizes input voltage ripple, suppresses input voltage spikes and provides a stable system rail for the device. A 4.7µF or larger input capacitor is required. The output capacitor value can range from 10µF up to more than 47µF. The recommended typical output capacitor value is 10µF. Values over 47µF may degrade the converter's regulation loop stability. A feed forward capacitor is required for best transient performance.

Ceramic capacitors have a DC-Bias effect, which has a strong influence on the final effective capacitance. Choose the right capacitor carefully in combination with considering its package size and voltage rating. Ensure that the input effective capacitance is at least 3µF and the output effective capacitance is at least 5µF.

10.2.1.3 Application Performance Curves

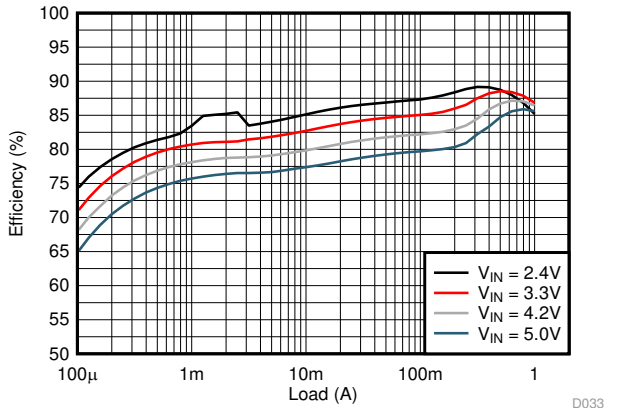
T_A = 25°C, V_{IN} = 5 V, V_{OUT} = 1.8 V, BOM = Table 3 unless otherwise noted.

10.2.1.3.1 TPSM82821 Performance Curves



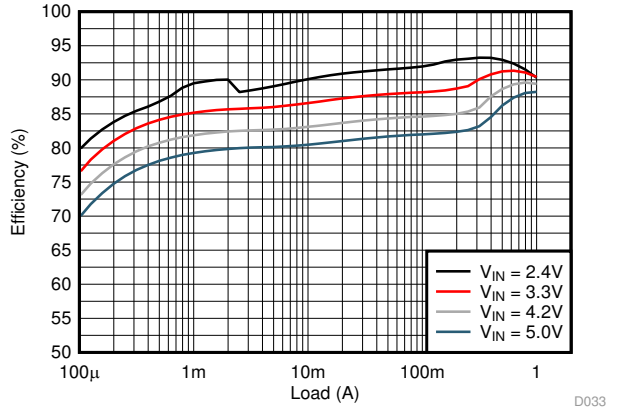
V_{OUT} = 0.6 V TPSM82821

Figure 6. Efficiency



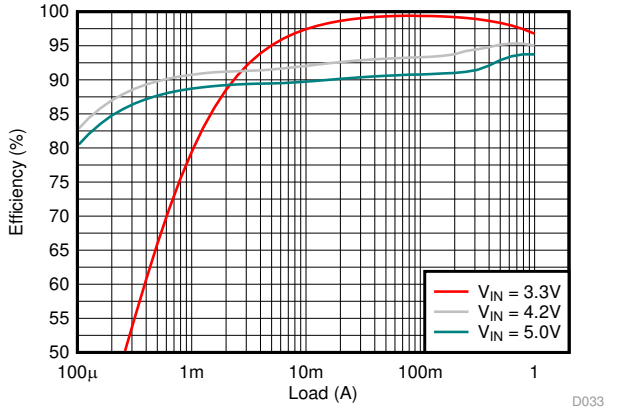
V_{OUT} = 1.2 V TPSM82821

Figure 7. Efficiency



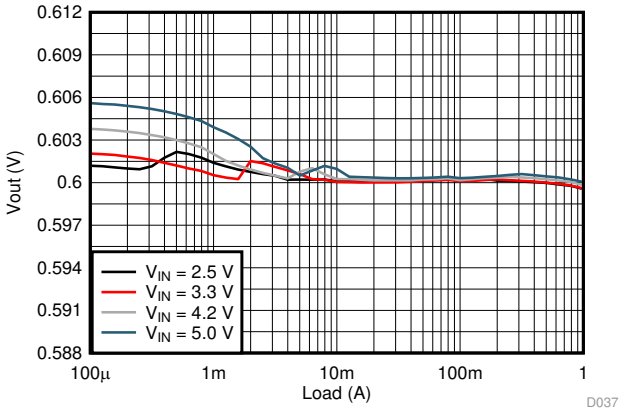
V_{OUT} = 1.8 V TPSM82821

Figure 8. Efficiency



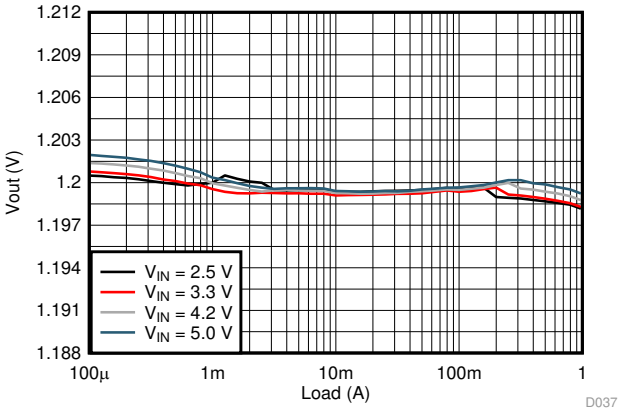
V_{OUT} = 3.3 V TPSM82821

Figure 9. Efficiency



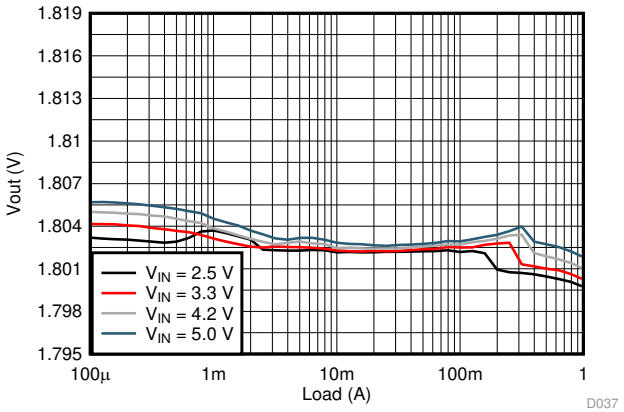
V_{OUT} = 0.6 V TPSM82821

Figure 10. Load Regulation



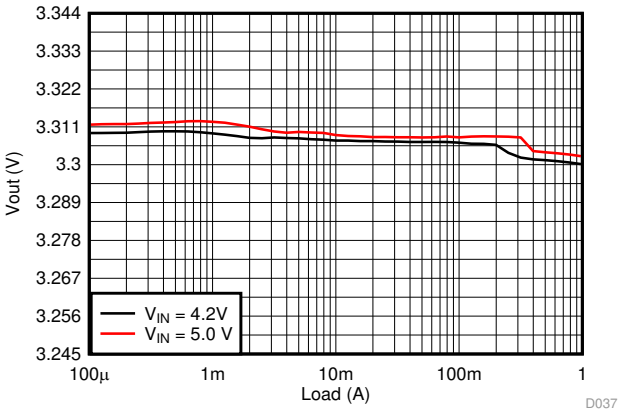
V_{OUT} = 1.2 V TPSM82821

Figure 11. Load Regulation



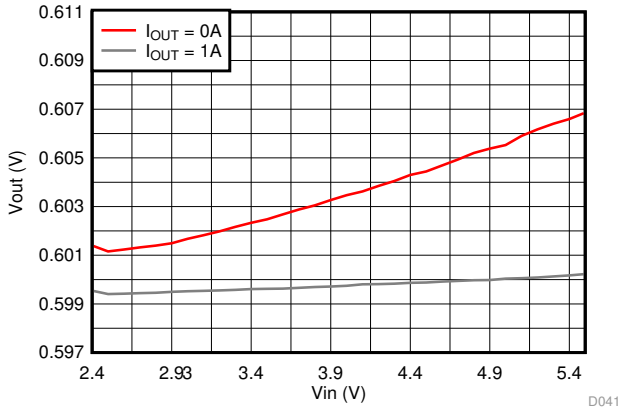
V_{OUT} = 1.8 V TPSM82821

Figure 12. Load Regulation



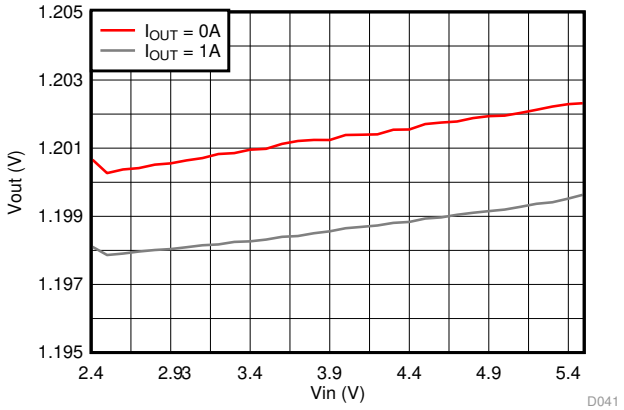
V_{OUT} = 3.3 V TPSM82821

Figure 13. Load Regulation



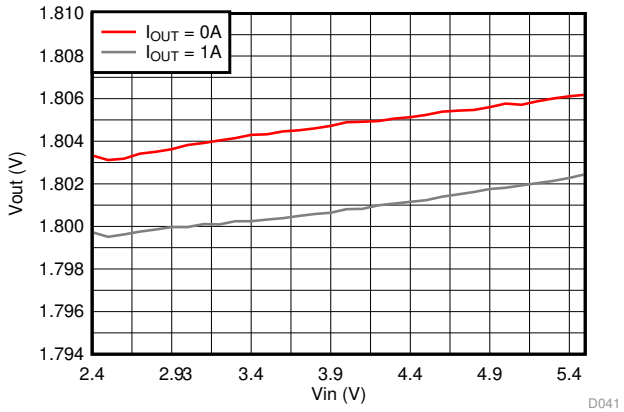
V_{OUT} = 0.6 V TPSM82821

Figure 14. Line Regulation



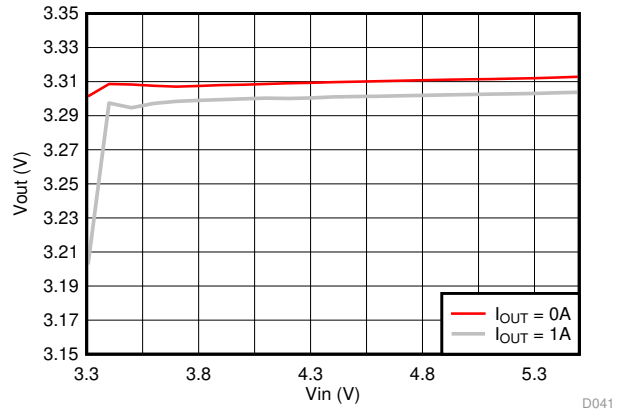
V_{OUT} = 1.2 V TPSM82821

Figure 15. Line Regulation



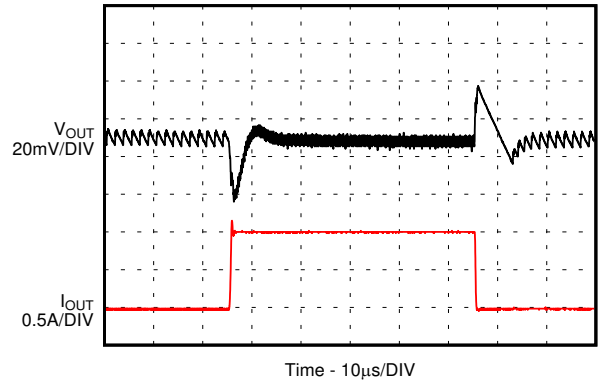
V_{OUT} = 1.8 V TPSM82821

Figure 16. Line Regulation



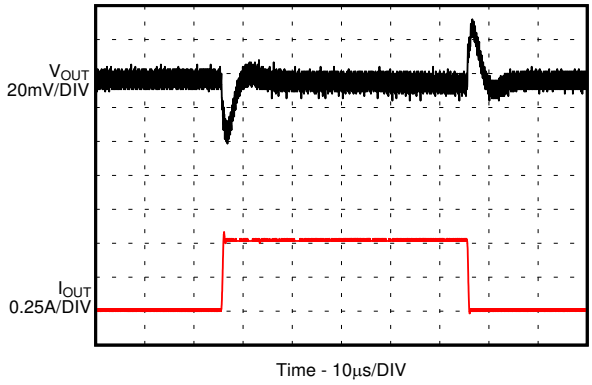
V_{OUT} = 3.3 V TPSM82821

Figure 17. Line Regulation



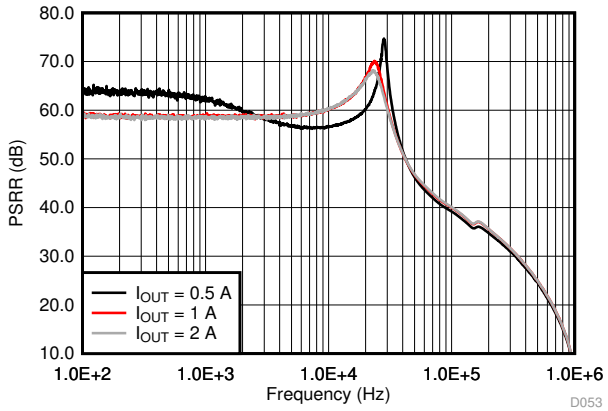
I_{OUT} = 0 A to 1 A | Slew Rate = 2 A/µs | TPSM82821

Figure 18. Load Transient



I_{OUT} = 0.5 A to 1 A | Slew Rate = 2 A/µs | TPSM82821

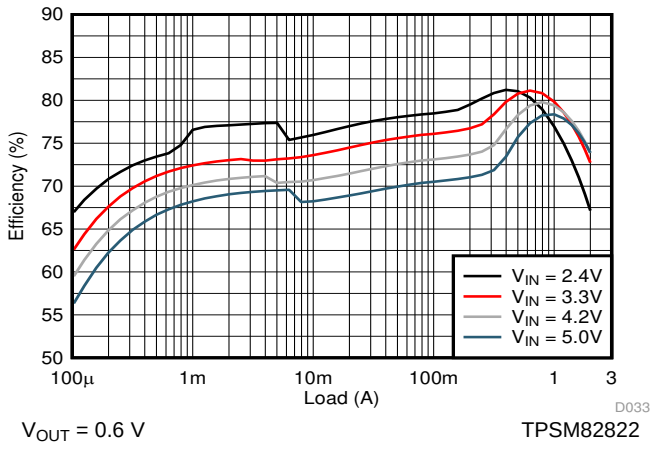
Figure 19. Load Transient



TPSM82821

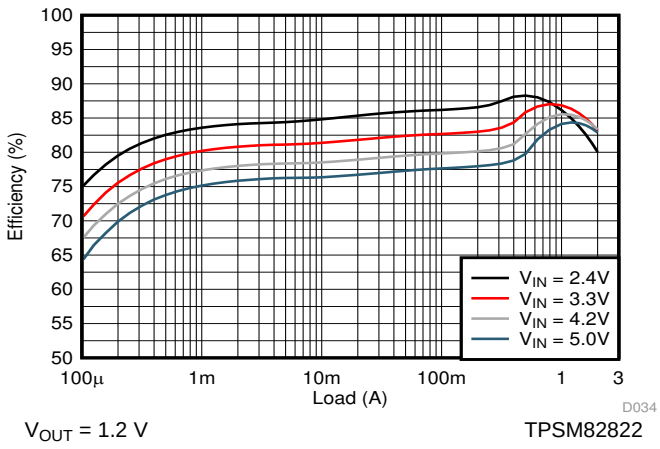
Figure 20. Power Supply Rejection Ratio (PSRR)

10.2.1.3.2 TPSM82822 Performance Curves



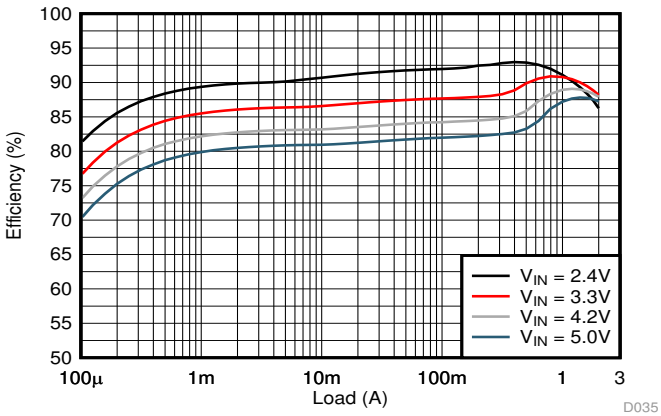
V_{OUT} = 0.6 V TPSM82822

Figure 21. Efficiency



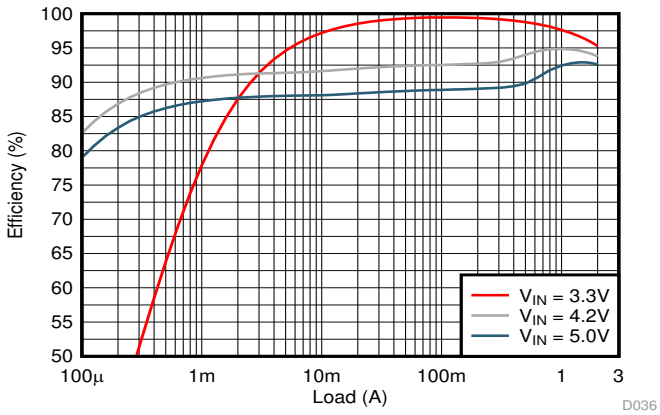
V_{OUT} = 1.2 V TPSM82822

Figure 22. Efficiency



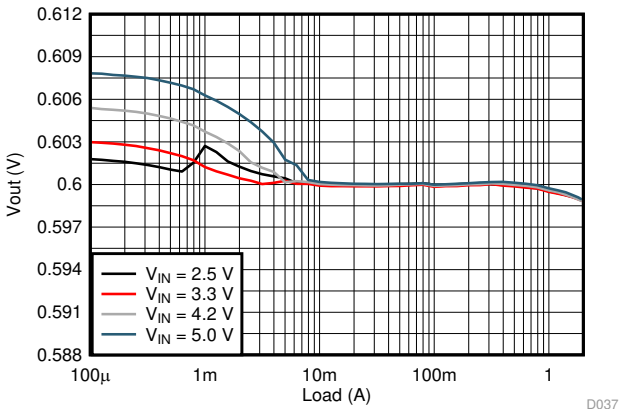
V_{OUT} = 1.8 V TPSM82822

Figure 23. Efficiency



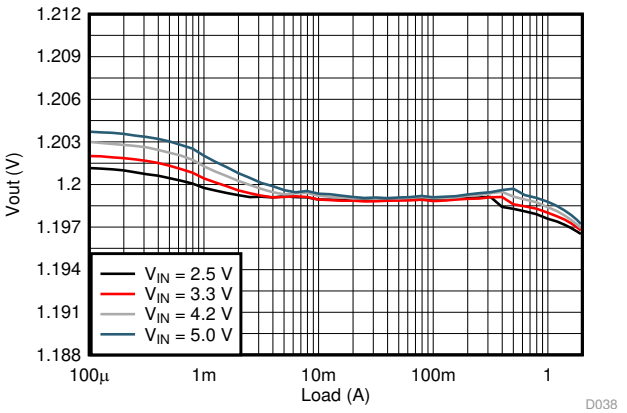
V_{OUT} = 3.3 V TPSM82822

Figure 24. Efficiency



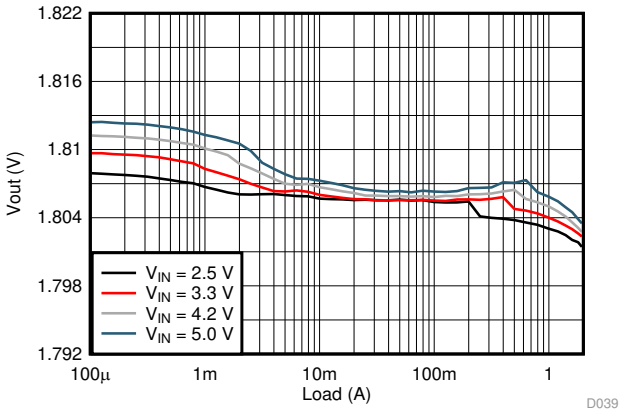
V_{OUT} = 0.6 V TPSM82822

Figure 25. Load Regulation



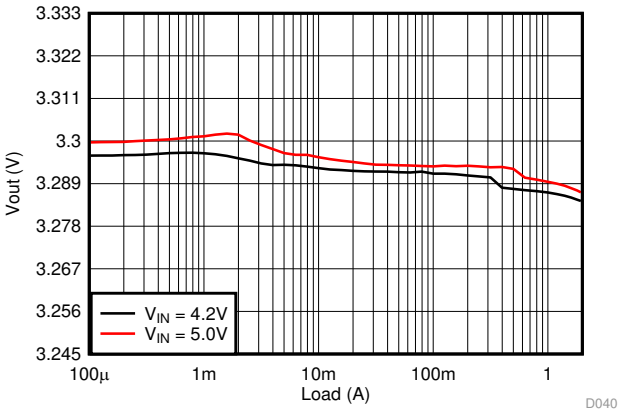
V_{OUT} = 1.2 V TPSM82822

Figure 26. Load Regulation



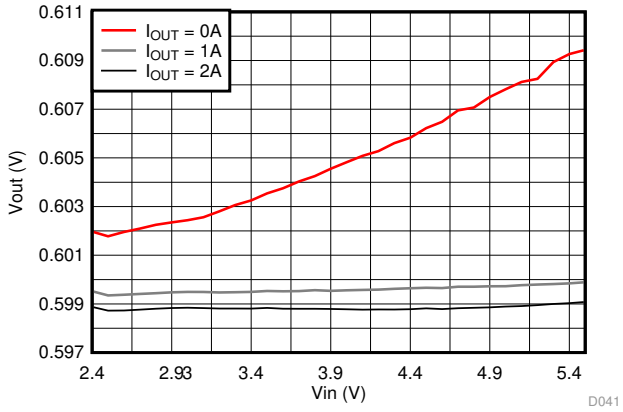
V_{OUT} = 1.8 V TPSM82822

Figure 27. Load Regulation



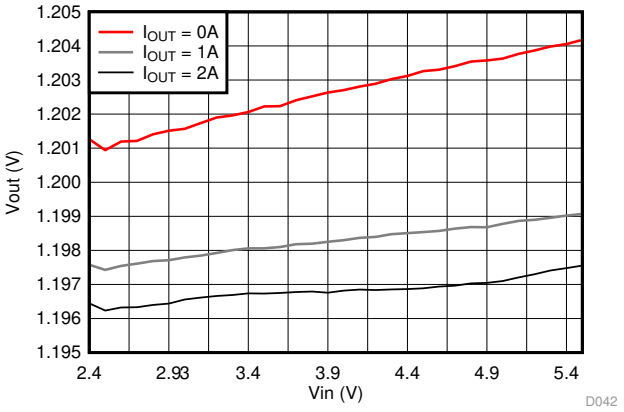
V_{OUT} = 3.3 V TPSM82822

Figure 28. Load Regulation



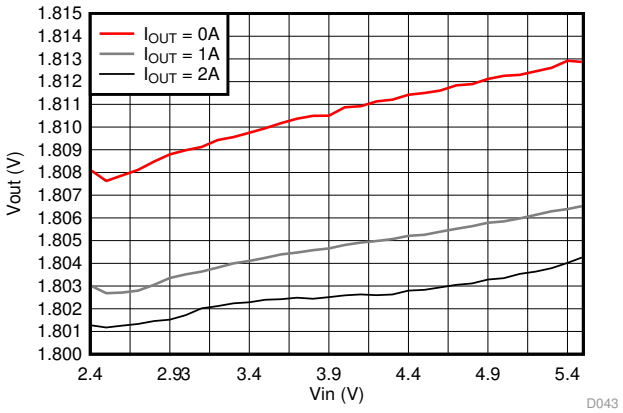
V_{OUT} = 0.6 V TPSM82822

Figure 29. Line Regulation



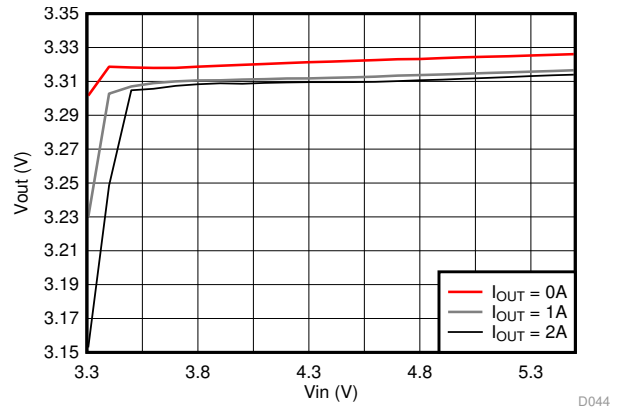
V_{OUT} = 1.2 V TPSM82822

Figure 30. Line Regulation



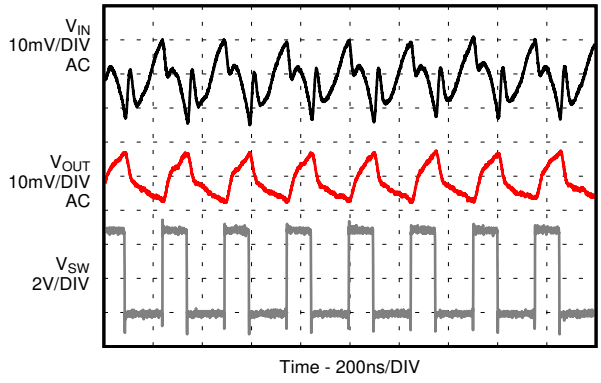
V_{OUT} = 1.8 V TPSM82822

Figure 31. Line Regulation



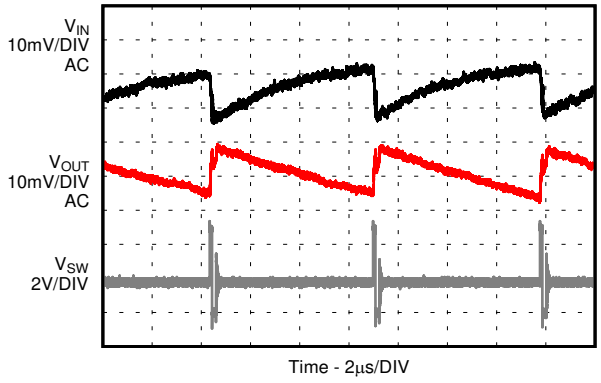
V_{OUT} = 3.3 V TPSM82822

Figure 32. Line Regulation



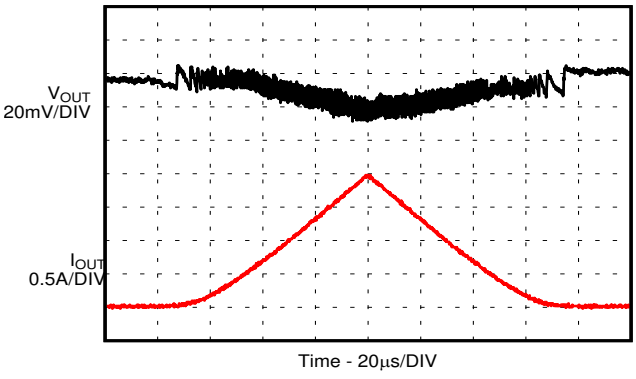
I_{OUT} = 2 A TPSM82822

Figure 33. Input and Output Ripple in PWM Mode



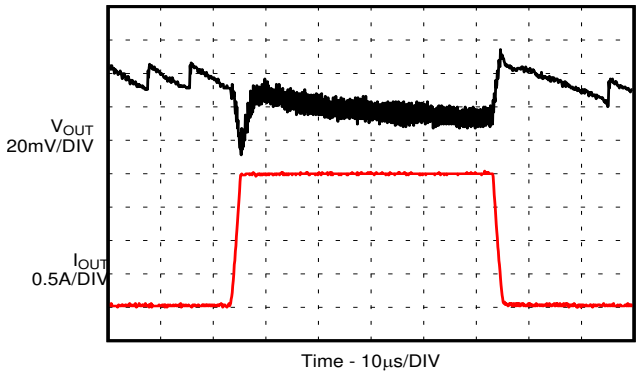
I_{OUT} = 25 mA TPSM82822

Figure 34. Input and Output Ripple in PSM Mode



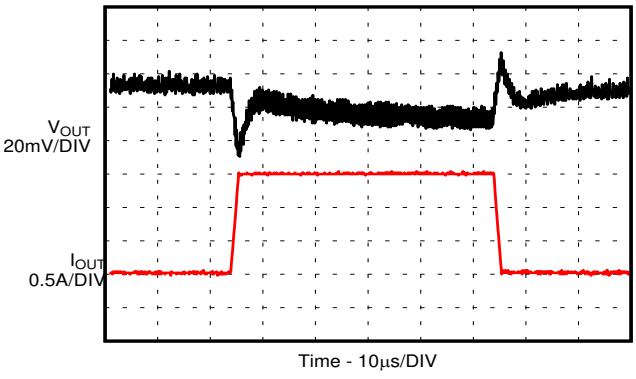
I_{OUT} = 25 mA to 2 A TPSM82822

Figure 35. Load Sweep



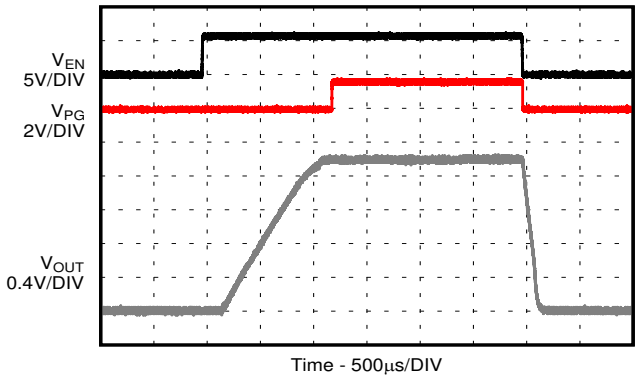
I_{OUT} = 0 A to 2 A Slew Rate = 2 A/µs TPSM82822

Figure 36. Load Transient



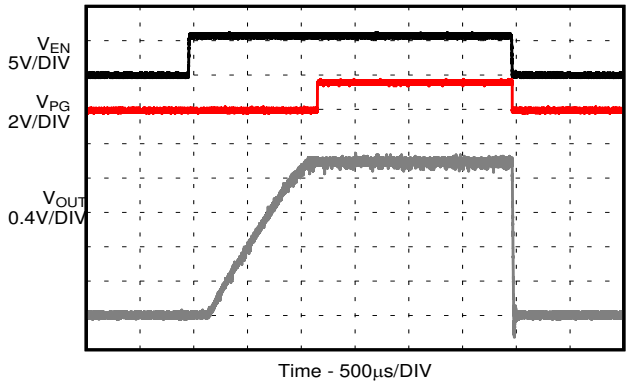
I_{OUT} = 0.5 A to 2 A Slew Rate = 2 A/µs TPSM82822

Figure 37. Load Transient



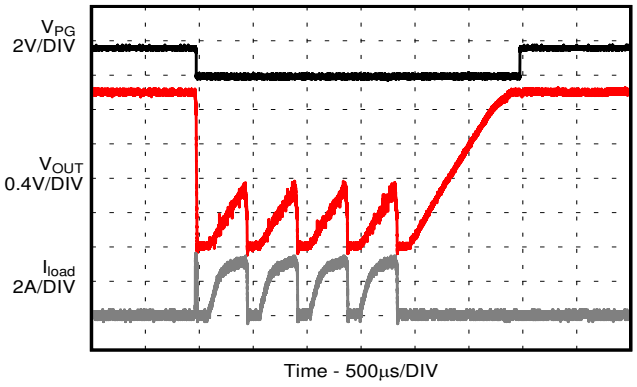
I_{OUT} = no load TPSM82822

Figure 38. Startup / Shutdown without Load



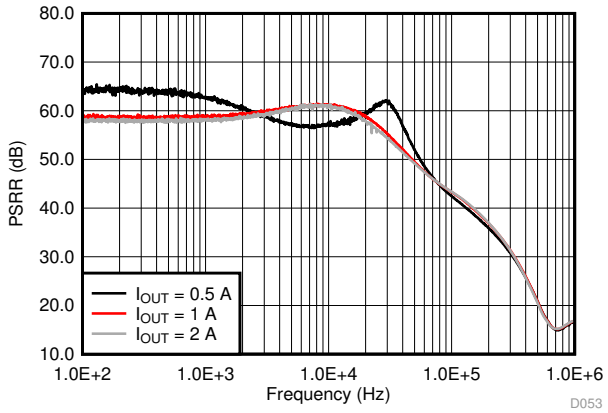
I_{OUT} = 2 A TPSM82822

Figure 39. Startup / Shutdown with Resistive Load



TPSM82822

Figure 40. Short Circuit, HICCUP Protection Entry / Exit



TPSM82822

Figure 41. Power Supply Rejection Ratio (PSRR)

11 Power Supply Recommendations

The devices are designed to operate from an input supply voltage range between 2.4V and 5.5V. The average input current of the TPSM8282x is calculated as:

$$I_{IN} = \frac{1}{\eta} \times \frac{V_{OUT} \times I_{OUT}}{V_{IN}} \quad (6)$$

Ensure that the power supply has a sufficient current rating for the application.

12 Layout

12.1 Layout Guidelines

- It is recommended to place all components as close as possible to the IC. Specially, the input capacitor placement must be closest to the VIN and GND pins of the device.
- Use wide and short traces for the main current paths to reduce the parasitic inductance and resistance.
- Refer to Figure 42 for an example of component placement, routing and thermal design.
- The recommended land pattern for the TPSM8282x is shown at the end of this data sheet. For best manufacturing results, it is important to create the pads as solder mask defined (SMD). This keeps each pad the same size and avoids solder pulling the device during reflow.

12.2 Layout Example

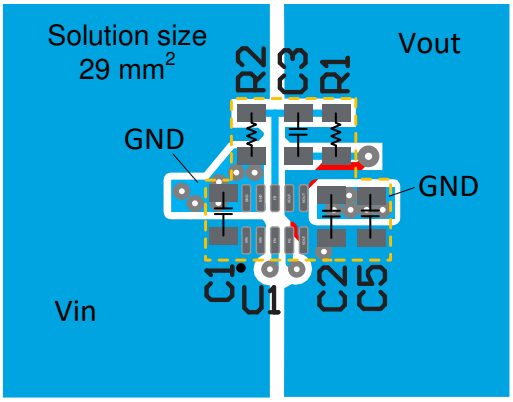


Figure 42. TPSM8282x PCB Layout

12.3 Thermal Consideration

The TPSM8282x module temperature must be kept less than the maximum rating of 125°C. Three basic approaches for enhancing thermal performance are listed below:

- Improve the power dissipation capability of the PCB design.
- Improve the thermal coupling of the component to the PCB.
- Introduce airflow into the system.

To estimate the approximate module temperature of the TPSM8282x, apply the typical efficiency stated in this datasheet to the desired application condition to compute the module's power dissipation. Then calculate the module temperature rise by multiplying the power dissipation by its thermal resistance. For more details on how to use the thermal parameters in real applications, see the application notes: SZZA017 and SPRA953.

13 Device and Documentation Support

13.1 Device Support

13.1.1 Third-Party Products Disclaimer

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13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *TPSM82821EVM-005 Evaluation Module*, SLVUBG0
- *TPSM82822EVM-005 Evaluation Module*, SLVUBG0

13.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

13.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.5 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.6 Trademarks

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13.7 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.8 Glossary

SLYZ022 — *TI Glossary*.

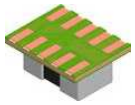
This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

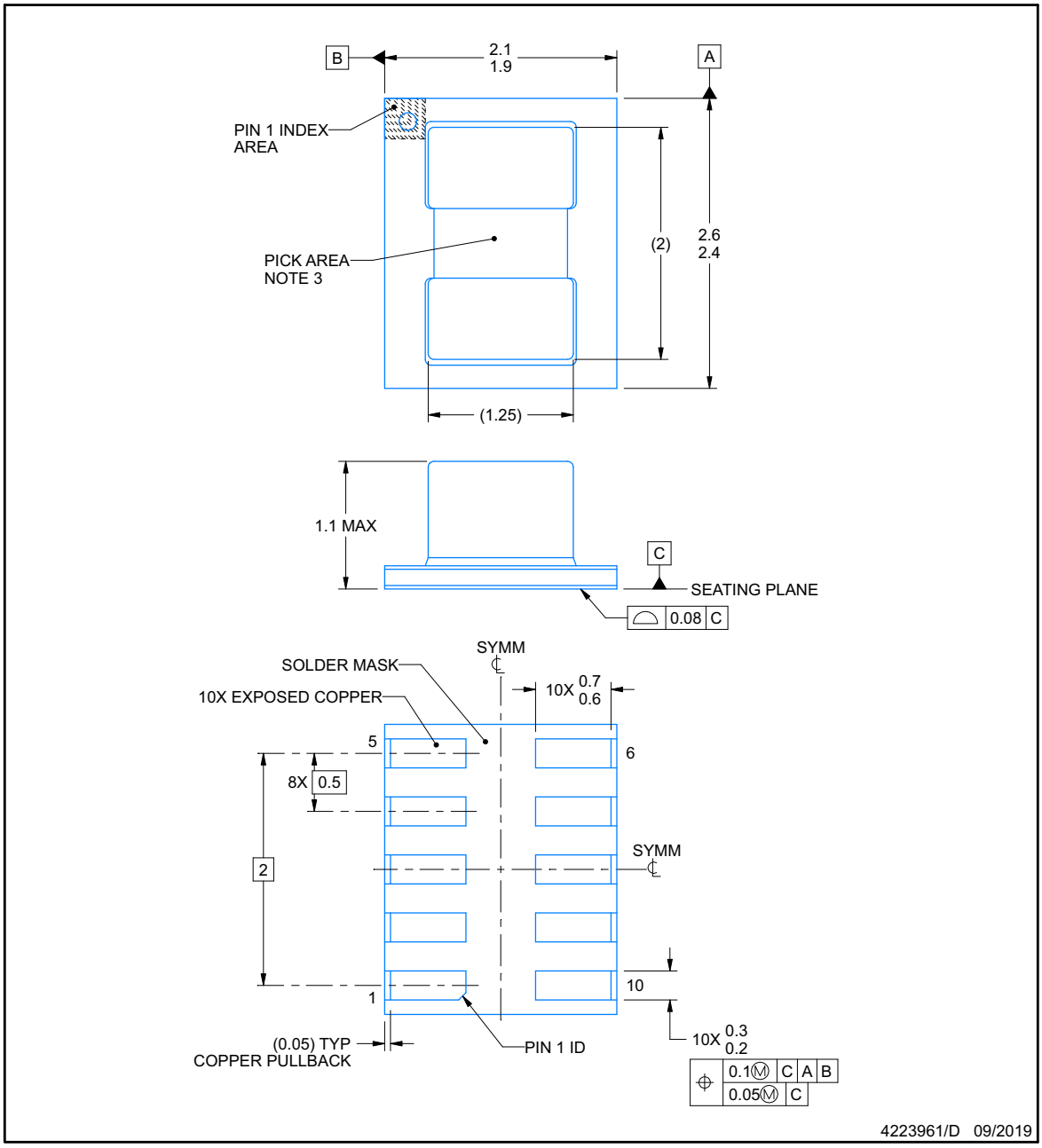
PACKAGE OUTLINE

SIL0010D



uSIP™ - 1.1 mm max height

MICRO SYSTEM IN PACKAGE



MicroSiP is a trademark of Texas Instruments

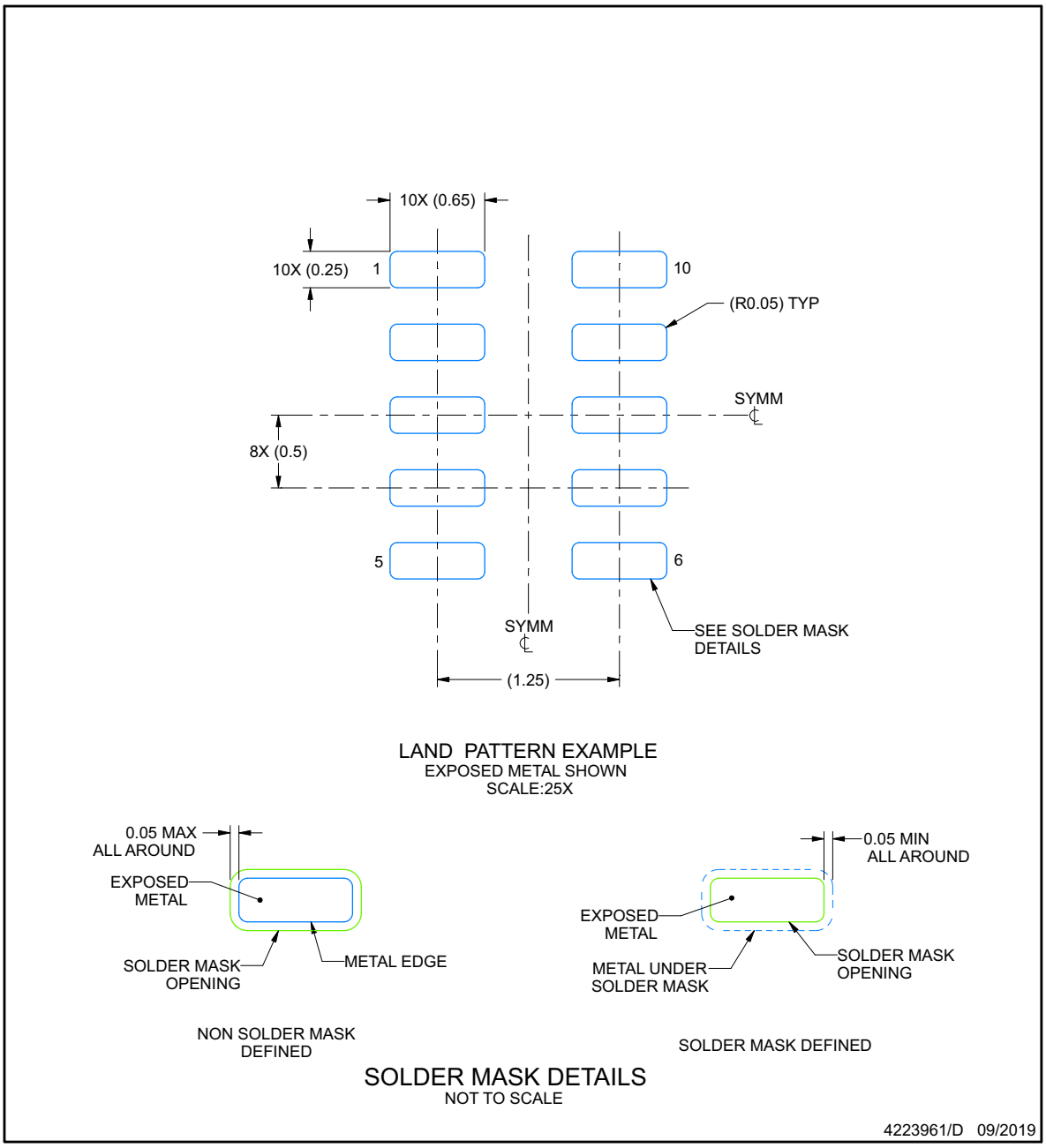
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Pick and place nozzle ∅ 0.33 mm or smaller recommended.

EXAMPLE BOARD LAYOUT

SIL0010D — **uSIP™ - 1.1 mm max height**

MICRO SYSTEM IN PACKAGE



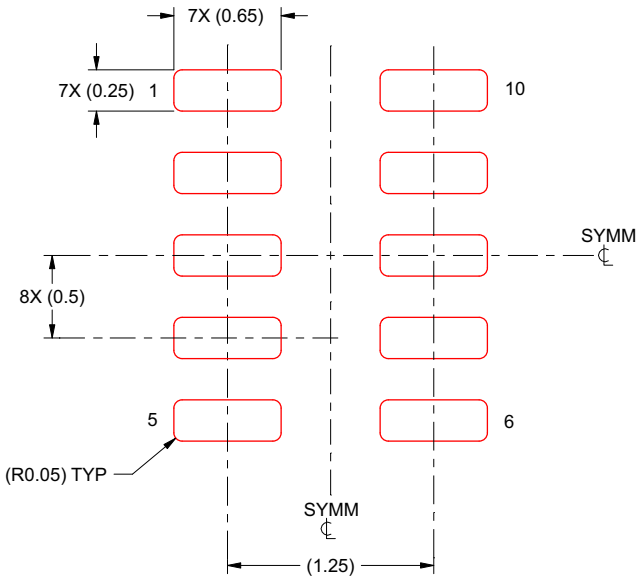
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

SIL0010D — **uSIP™ - 1.1 mm max height**

MICRO SYSTEM IN PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:25X

4223961/D 09/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPSM82821SILR	PREVIEW	uSiP	SIL	10	3000	RoHS (In Work) & Green (In Work)	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	GA	
TPSM82822SILR	PREVIEW	uSiP	SIL	10	3000	Green (RoHS & no Sb/Br)	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	G9	
XPSM82822SILR	ACTIVE	uSiP	SIL	10	3000	Green (RoHS & no Sb/Br)	ENEPIG	Level-2-260C-1 YEAR	-40 to 125	XX	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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